SYNOPSYS®

Purple 100 Program

Fastrack to SoC Design Career

The Next-generation SoC Design Education

Synopsys Trainers with over 10 years of professional experience
Instructor-led courses in virtual classrooms
50% hands-on labs on Cloud
The latest Synopsys tools with individual licenses

E-learning | Instructor-led | Cloud Practice

Fundamental Module (Self-learning)

ASIC Design Flow, CMOS Basics, Linux Basics, TCL/Tk

Module A — SoC Frontend Design (Lecture + Lab)

7/25—8/5
NT$24,000

Week1 5 DAYS Synthesis, Formal Verification & Verification Basics
Week2 4 DAYS UPF & STA

Module B — Physical Design (Lecture + Lab)

8/8—8/12
NT$12,000

Week3 5 DAYS APR Basics & APR Advanced

Module C — Design Verification (Lecture + Lab)

8/15—8/26
NT$24,000

Week4 5 DAYS Verification Advanced
Week5 5 DAYS FPGA Prototyping (*on-site)

Module D — Design For Test (Lecture + Lab)

8/22—8/26
NT$12,000

Week5 5 DAYS DFT

Module E — Digital Instance (Lecture + Lab)

8/26
Free of Charge

Week5 1 DAY Digital Instance SaaS for RTL-to-Sign-off

»Sign up for 2 or more modules and get 15% tuition off.
»Get 50% tuition refund if pass all module requirements.

Eligibility

- Students in master or Ph.D. programs in EE, CS, or EECS
- Familiar with basics of VLSI design, digital design, and Linux

Opening Ceremony 7/20

Commencement & Job Match 9/8

APPLY NOW

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